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Improvement on Address Discharge Characteristics for Overall Subfield Time Using Additional Scan Voltage in AC PDP

JOON-YUB KIM,[1] YEON TAE JEONG,[2]
AND BYUNG-GWON CHO[2,*]

[1]Department of Electronics Engineering, College of Electronics & Information Engineering, Sejong University, Seoul, Korea
[2]Department of Display Engineering, College of Engineering, Pukyong National University, Busan, Korea

The address discharge time lags are investigated in each subfield time in AC PDP and shortened by changes in the amplitude of the additional scan voltage during total subfield time under the stable address voltage margin range. During the reset period, the reset discharge is produced by applying the high positive-going ramp voltage and the wall charge in a cell is generated. That wall charge plus the external address voltage induce the address discharge. In the first subfield time, the address discharge is fast produced than the other subfield times because the wall charge are much remained by the high positive-going ramp voltage during the reset period. Meanwhile, from the second to last subfield, the address discharge production time is gradually delayed due to the dissipation of the wall charge in a cell. In this study, the address discharge time lags are measured in each subfield time and the modified driving method to shorten the total address discharge time is proposed by applying the different additional scan voltages in each the subfield time.

Keywords Address discharge; Wall charge; Subfield time; Plasma display panel; PDP

1. Introduction

The address-display-separated (ADS) driving method that one TV frame time (16.67 ms) is separated into the several subfield times, over eight, has been usually used in the AC plasma display panel. One TV screen in this driving method is completed by the selective combination of the several subfields, then the each subfield is composed of the reset, address, and sustain period. The reset period initialize the wall charge state in all cells by the high positive-going ramp voltage, and the address period is the time for selecting the cell to express in the screen by the scan and address pulses. The screen can be displayed by the alternating plasma discharge in the sustain period at the selected cells after the address period [1]. However, according to the ADS driving method of a plasma display panel, since the entire writing operation should be scanned to the individual cells in the longitudinal

*Address correspondence to Prof. Byung-Gwon Cho, Department of Display Engineering Pukyong National University, Busan 608-737, Korea (ROK). E-mail: bgcho@pknu.ac.kr

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direction, the address period is increased as long as the number of cells, as a result, the disadvantage that the shortened sustain period caused the low luminance is found [2]. In other words, it is possible to increase the luminance by the increase of the sustain period if the address period of each subfield time can be shortened. To shorten the address period, the applying time of the scan and address pulses to each cell should be reduced. However, the reduction of the scan and address time reaches the limit because the reduction of the address pulse-width induce the unstable address discharge or the discharge failure after applying the shortened scan and address pulses [3]. The address discharge delay time is defined the period that the plasma discharge is produced stably after applying the scan and address pulses, therefore, the total address time can be shortened if this delay time can be reduced. As the address discharge delay time is determined by the amount of the wall charge produced by the reset period plus the amplitude of the externally applied voltage, a lot of wall charges are accumulated in cells or the amplitude of the externally applied voltage should be increased to produce the address discharge fast and shorten the address time. However, as it has a limitation that the wall charges are accumulated by the positive-going ramp waveform during a reset period, the externally applied voltage is needed to increase [4, 5]. Also, because the wall charges in a cell are only accumulated by the positive-going ramp waveform during a reset period in the first subfield time, the accumulated wall charges are dissipated as time passed and the address discharge delay time is gradually increased from the second to final subfield time.

In this study, the address discharge delay times is first investigated when the additional scan voltage is applied in each subfield time, and the address discharge characteristics is also measured when applying the additional scan voltage with the various amplitude in each subfield time. Considering the experimental results and the address voltage margin, the additional scan voltage with different amplitude is applied after the second subfield time and the address discharge delay time is shortened.

2. Experiment

2.1. Conventional Driving Method

Figure 1 shows the conventional driving waveforms including the main (a) and subsidiary reset (b) waveform during one subfield time. In the subfield time, the time was divided into the reset period with the positive-going and negative-going ramp waveform on the Y electrode, the address period applying the pulses to the Y and A electrodes, and the sustain period applying the pulses alternately to the X and Y electrodes. The X waveform indicated the driving waveform applying to the front common X electrodes in AC PDP and the Y waveform showed the driving waveform applying to the Y electrodes with parallel line to the X electrode in Figure 1. While lines of X electrodes were commonly connected, Y electrodes were separated into the individual line for the sequential scanning process, and A electrodes was the vertical directional lines of the X and Y electrodes at the rear side. One subfield time consisted of the reset, address, and sustain period, respectively. In a reset period, the wall charge was accumulated on three electrodes and redistributed to facilitate the production of the address discharge in a cell. When a scan pulse on the Y electrode and an address pulse on the A electrode were applied simultaneously during an address period, an address discharge was produced and the wall charge distribution changed at a selected cell for displaying. During the sustain period, the square pulses alternately applied to the

Table 1. Voltage levels applied to driving waveforms in Figure 1

V_{set}	V_s	V_b	V_{scl}	V_a
175	175	150	−50	50

X and Y electrodes and the sustain discharge were produced in succession at the selected or an address discharged cell (Table 1).

Figure 1(a) shows the driving waveform applied to the AC PDP in one subfield time containing the main reset waveform, and Figure 1(b) shows the driving waveform containing the subsidiary reset waveform. In general, the main reset waveform of Figure 1(a) was only used in the first subfield time and the subsidiary reset waveforms of Figure 1(b) were used

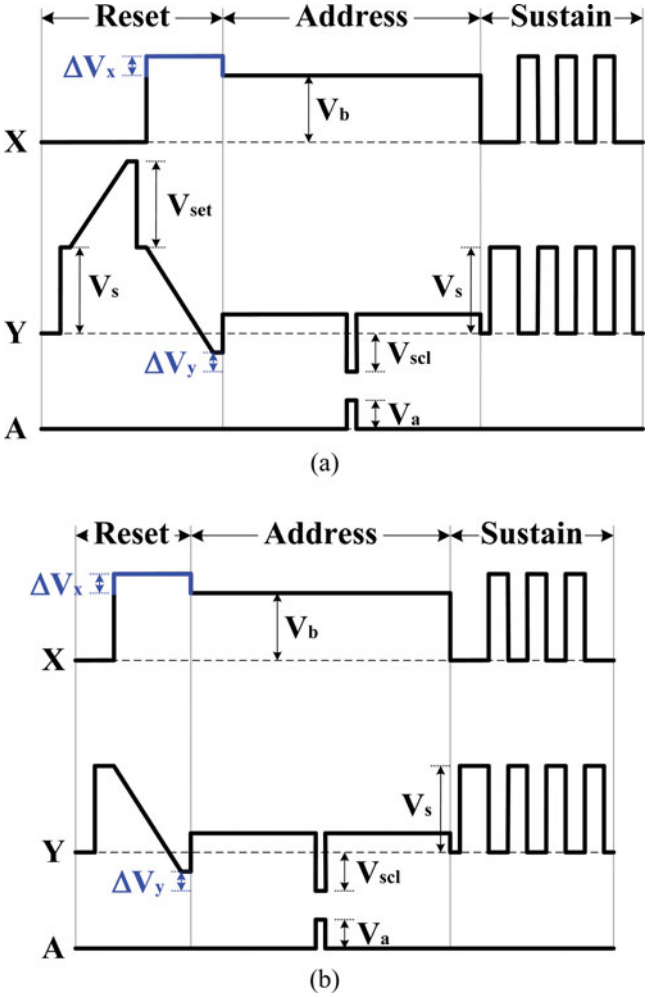

Figure 1. Conventional driving waveforms with main (a) and subsidiary reset waveform (b) under constant additional scan voltage applied to Y electrode.

in the other subfield times [6]. As the positive-going ramp waveform of the main reset waveform was applied to the Y electrodes, the plasma discharge was produced by the high reset voltage and the wall charges were accumulated in a cell. Meanwhile, the subsidiary reset waveform has only the negative-going ramp waveform without the positive-going ramp waveform because that utilized the accumulated wall charge in the previous subfield time. However, it is natural that the address discharge characteristics were weak in the subfield time adopting the subsidiary reset waveform due to the dissipation of the accumulated wall charge in process of time. To improve the address discharge characteristics, the main reset waveform could be adopted in overall subfield times but the positive-going ramp waveform of the main reset waveform induce the low contrast ratio due to high background luminance by the reset discharge. In addition, the sustain period for displaying the screen could be decreased due to the long time of the positive-going ramp waveform and the luminance was also decreased.

In recent years, the method of applying the additional scan voltage (ΔV_y) to the Y electrode at the time of the scan procedure had been proposed and adopted to the driving waveform [7]. The additional scan voltage meant the voltage difference between the negative-going ramp voltage level of the Y electrode during a reset period and the scan voltage level during an address period. As the address discharge characteristics was determined by the sum of the wall voltage by the accumulated wall charge in a cell and externally applied voltage, the application of the additional scan voltage functions as increase of the externally applied voltage and consequently the address discharge delay time can be reduced.

2.2. Measurement of Address Discharge

The address discharge delay times were measured during an address period of each subfield time when the scan pulse including the additional scan voltage (ΔV_y) of 30 V and address pulse were applied to AC PDP as shown in Figure 2. It was found that the address discharge at the first subfield time was the fastest produced and the production times of the address

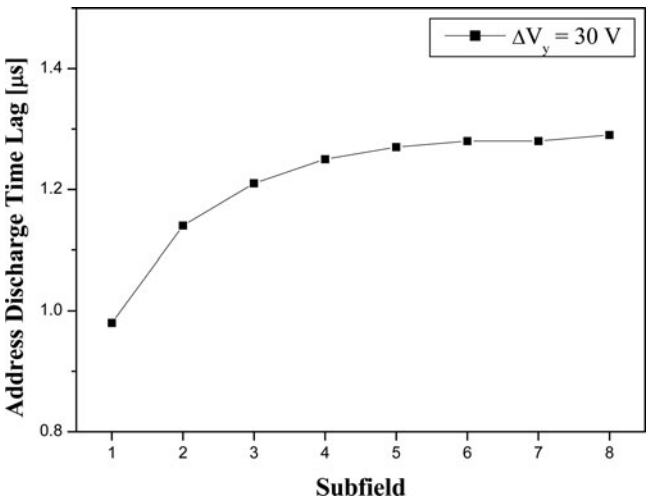

Figure 2. Measured address discharge time lags for each subfield time when main reset waveform is applied to only the first subfield in the conventional driving waveform.

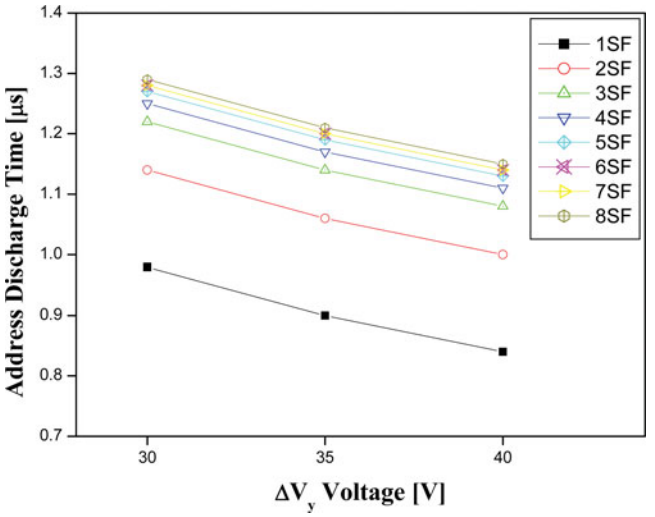

Figure 3. Measured address discharge time lags with changing amplitude of additional scan voltage during address period in each subfield (SF).

discharge were gradually delayed in the course of time. Due to the address discharge time lags, the reduction of the scan and address pulse-width in each line reach the limit and that caused the increase of the total address period. Reviewing the driving waveform in Figure 1, the wall charge and priming particle were produced in a cell by the positive-going ramp waveform during the first subfield time. Therefore, the address discharge in the other subfield times utilized the wall charge and priming particle produced in the first subfield time because the wall charge could not be again produced by the subsidiary reset waveform. However, as the produced wall charge and priming particle were dissipated as time passed, the address discharge delay time was also increased gradually. If the additional scan voltage was increased as much as the amount of the erased wall charge, the address discharge delay time could be reduced.

Figure 3 shows the measured address discharge delay time with changes in the amplitude of the additional scan voltage during an address period. When the additional scan voltage was 30 V, the address discharge time was delayed to 1.3 μs in the case of the eighth subfield. As shown in Figure 3, it was found that the address discharge delay time could be reduced when the additional scan voltage was high. Therefore, if the additional scan voltage was set 40 V, the address discharge delay time in the overall subfield time could be reduced under 1.2 μs. However, when the additional scan voltage was set 40 V even in the first and second subfield time, the misfiring discharge could be produced because that condition was out of the voltage margin as shown in Figure 4. The inside of line in the graph of the address voltage margin indicated the normal production of the address discharge, while the outside meant the abnormal or no address discharge. The vertical axis in Figure 4 was the address voltage and horizontal axis was the amplitude of the additional scan voltage. The address voltage margin after the third subfield was omitted as that was similar to the margin in the third subfield. Based on the experimental results in Figures 3 and 4, three kinds of the additional scan voltages were applied to the Y electrodes during the address period in each subfield time. That is, to improve address discharge characteristics,

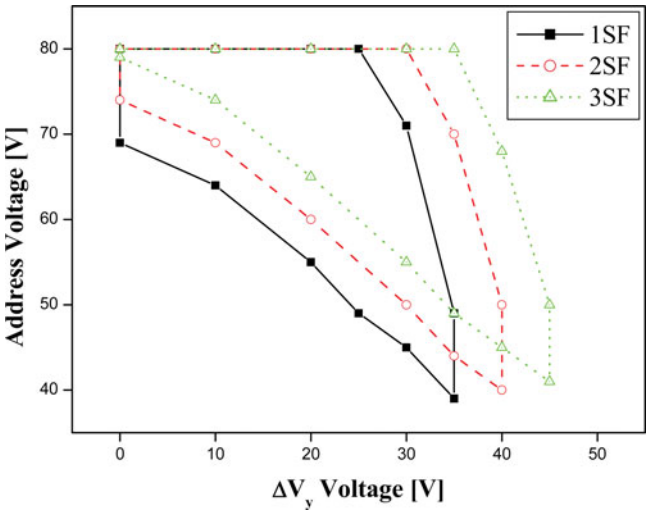

Figure 4. Address voltage margins with changing in additional voltage of the first, second, and the other subfields.

the additional scan voltage of 30 V should be applied to the Y electrode in the first subfield time, 35 V in the second subfield time, and 40 V from the third to the eighth subfield times.

3. Modified Driving Method

The modified driving waveform was proposed in Figure 5 that the different additional scan voltages were applied based on the address discharge time lags and the address voltage margin of Figures 3 and 4. Comparing to the driving waveform of Figure 1, the additional scan voltage of the first subfield time was the same as 30 V, while 35 V was applied in the second subfield time and 40 V was applied from the third to eighth subfields. As a result, in comparison with the conventional address discharge time lag of Figure 2, it was found that the address discharge delay time could be reduced after the second subfield time as shown

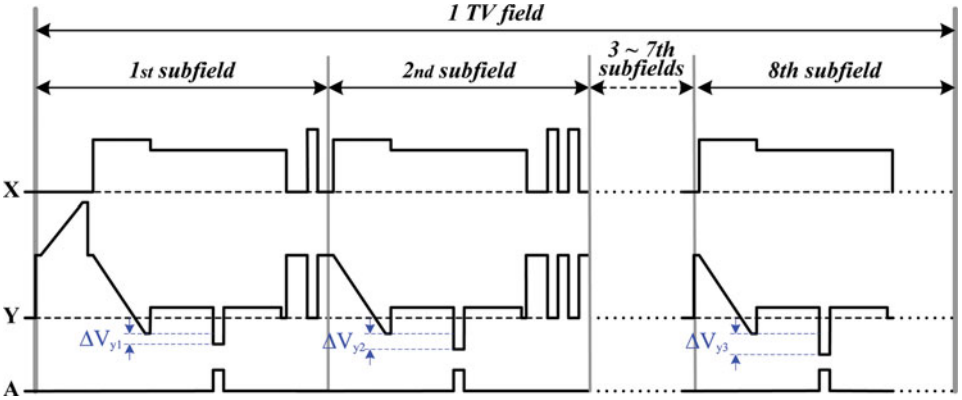

Figure 5. Modified total driving waveform applying different additional scan voltage during address period in each subfield time.

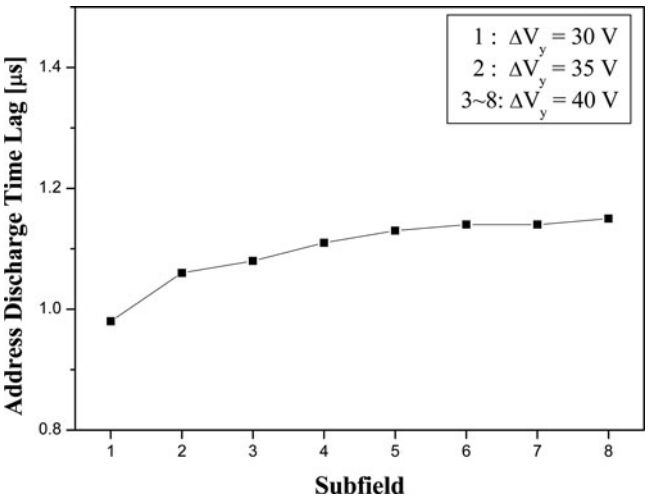

Figure 6. Modified total driving waveform applying different additional scan voltage during address period in each subfield time.

in Figure 6. When adopting the conventional driving method, the longest address discharge delay time was 1.3 μs in Figure 2. However, when adopting the modified driving method, the address discharge delay time could be reduced to 1.15 μs. We will calculate how much it can be reduced total address discharge time if the scan pulse-width was shortened to 1.15 μs from 1.3 μs. Let's assume the number of the horizontal cell were 1024 and the vertical cell were 768 in HD resolution of AC PDP, the scan and address procedure was implemented to vertical 768 cell as the scan pulse was applied in the vertical direction in AC PDP. Therefore, the total address time could be calculated as following equation:

$$\text{Time} = \text{Ce} \times \text{Su} \times \text{Pw}$$

Where, Ce was the number of the cell in the vertical direction, Su was the number of the subfield, and Pw indicated an address pulse-width during an address period. In the conventional driving method, the total address time was needed $768 \times 8 \times 1.3\ \mu\text{s} = 7987\ \mu\text{s}$. That means the address time of 7.98 ms was occupied 47% for one TV frame time (16.67 ms). However, in the modified driving method, as the total address time could be reduced to $768 \times 8 \times 1.15\ \mu\text{s} = 7065\ \mu\text{s}$. That is, the address time could be reduced to 7 ms, 41% of one TV frame time. This reduced time can contribute to improve the luminance of AC PDP because the reduced time induce the increase in the sustain period.

4. Conclusion

As the address period is occupied almost a half time of one TV frame, the sustain period is insufficient for the luminance of AC PDP. In a measurement of each address discharge delay time during a subfield time in one TV frame time, the address discharge delay times after the first subfield time were increased as the wall charge for the address discharge were only accumulated by the positive-going ramp waveform in the first subfield time. Therefore, the modified driving waveform applying the different additional scan voltages in each subfield time was proposed to shorten the address discharge delay time. As a result, the total address time could be reduced about 6%, 900 μs, based on the eight subfields time

system. This reduction time can utilize to increase the sustain period for improvement of the luminance and contribute to the discharge stability in the reset period.

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